Process Technology for the Monolithic Integration of Low-Temperature Polysilicon and Metal-Oxide Thin-Film Transistors

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Offering the high current-drive of a low-temperature polysilicon (LTPS) thin-film transistor (TFT) and the low off-state current of a metal-oxide (MO) TFT, the monolithic integration of p-type LTPS and n-type MO TFTs has attracted much attention for implementing complementary circuits in displays and other applications [1]. However, such monolithic integration presents several incompatibility issues regarding materials and processes, for example, hydrogen (H) cross-contamination, contact treatment, and metallization: (i) while LTPS TFTs demand H for trap-passivation, the H presented in the channel region of an MO TFT could result in a negative shift of threshold voltage or even electrical shorting of the channel. Thus, the presence and distribution of H in an MO TFT must be carefully managed [1]. (ii) During the back-end processes, the treatment based on hydrofluoric (HF) acid used to remove the native oxide in the contacts to an LTPS TFT leads to aggressive etching of indium-gallium-zinc oxide (IGZO), a popularly deployed MO semiconductor; consequently, the MO needs to be properly protected. (iii) Different conductive source/drain electrodes are needed to form good ohmic contacts to LTPS and MO, thus making it desirable to incorporate two separate conductor layers without incurring excessive process complexity. Presently addressed are approaches for resolving these issues.

Fluorination is investigated as a solution for protecting MO TFTs exposed to H-containing processes. The improved resilience against hydrogen-induced degradation of a fluorinated IGZO TFT is consistent with reduced incorporation of hydrogen in the active layer of the TFT [2].

A stacked-interconnect scheme is proposed to solve the integration issues arising from contact treatment and metallization [3]. The utility of this scheme is reflected in a narrow distribution of both the specific contact resistance and the performance of the fabricated TFTs. Complementary digital and analog circuit blocks using top-gate p-type LTPS and bottom-gate n-type IGZO TFTs are designed, fabricated, and characterized.

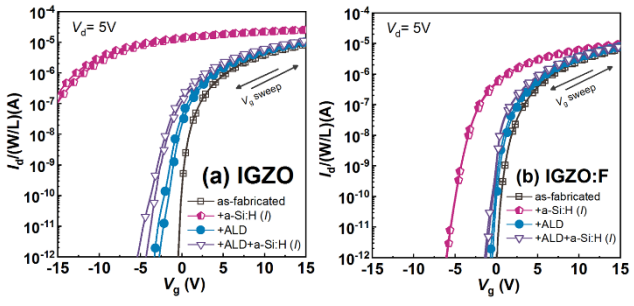

Fig. 1. The transfer characteristics of (a) IGZO and (b) IGZO:F TFT (as-fabricated); directly subjected to a-Si:H deposition (+exposure to H); covered with a 40-nm-thick ALD Al_2O_3 diffusion barrier (+ALD) and subsequently subjected to a-Si:H deposition (+ALD+exposure to H).

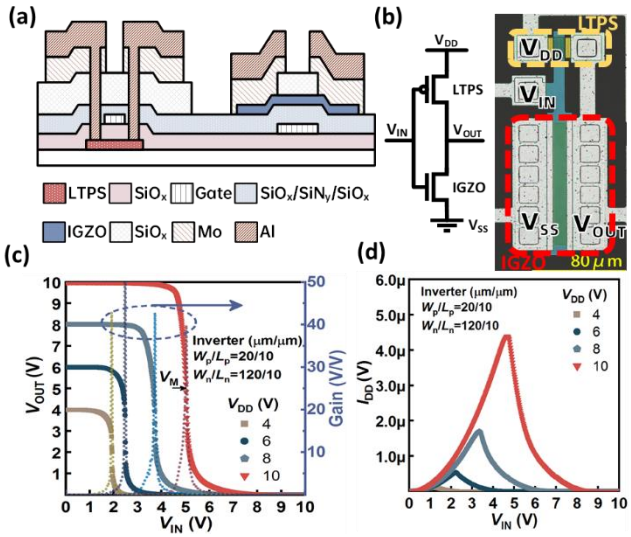

Fig. 2. Inverter circuit consisting of monolithically integrated p-type TG LTPS/HF+Al pull-up and n-type BG IGZO/Mo pull-down TFTs: (a) cross-section of the integrated TFTs using stacked-interconnect of Al-on-Mo. (b) Circuit diagram and optical image. (c) The voltage and (d) current transfer characteristics, also showing the dependence of the voltage gain on V_{IN}.

References

[1] T.-K. Chang, C.-W. Lin, and S. Chang, "39-3: Invited Paper: LTPO TFT Technology for AMOLEDs," *SID Symposium Digest of Technical Papers*, vol. 50, no. 1, pp. 545–548, Jun. 2019.

[2] S. Wang, R. Shi, J. Li, L. Lu, Z. Xia, H. S. Kwok, and M. Wong, "Resilience of Fluorinated Indium-Gallium-Zinc Oxide Thin-Film Transistor Against Hydrogen-Induced Degradation," *IEEE Electron Device Letters*, vol. 41, no. 5, pp. 729–732, 2020.

[3] S. Wang and M. Wong, "Stacked-Interconnect for Monolithic Integration of Low-Temperature Polysilicon and Amorphous Metal-Oxide Thin-Film Transistors," *IEEE Electron Device Letters*, vol. 42, no. 9, pp. 1331-1333, Sept. 2021.